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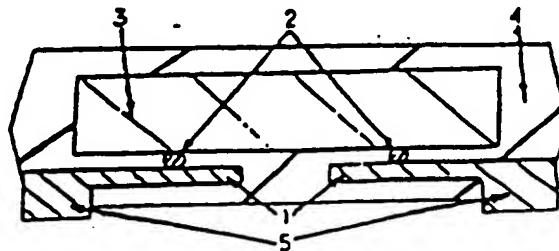
(5)【発明の名前】半導体装置

(6)【要約】

(目的) 半導体装置の面積縮小における実装密度を向上すること。

(構成) 半導体チップとそれに電気的に接続された内部リードを複数で封止した半導体装置であって、所述半導体装置の封止部周部の底面もしくは、上部から内部リードの一端を突出させも。

図1



それも。

〔0022〕これにより、又反、既存封止部の既存部から突出していたカギリードの部分だけ、又スベースを切り取るなり、他の部品等の実体に取り付けてたりすることができる。

〔0023〕次に、図5を用いて、本実用新型の半導体部のリードフレームについて説明する。

〔0024〕図5において、3Aは大きめの半導体チップ、3Bは小さめの半導体チップ、2Aは大きめの半導体チップと内部リード部分を包含するパンプ、2Bは大きめの半導体チップと内部リード部分を包含するパンプをそれぞれ示す。

〔0025〕図5に示すように、本実用新型の半導体部のリードフレームの形状は、フレームの中心附近から内部リードが斜め上に広がっている。

〔0026〕これにより、既存封止部の大きめの半導体チップである大きめの半導体チップ3Aを封止する場合でも、小さめの半導体チップ3Bを封止する場合でも、も半導体チップ3A、3Bのパッド位置を内部リード1上の接触可能位置に変更し、その位置にパンプ2A、2Bを設けることで半導体チップ3A、3Bと内部リード部分1とを固定できる。このパンプ部による内部リードと半導体チップとの電気的な接続はワイヤ接続ではなく、半導体部の内側で接続される。

〔0027〕すなわち、本実用新型のリードフレーム一つで多種の半導体チップを適用できる。

〔0028〕次に、本実用新型の他の実用例を図6と図7に示す。

〔0029〕図6に示す半導体部の形状は、前述の図1に示した半導体部の内部リード部分1とカギリード部分の形状をなくしたものであり、内部リードと外部リードを実用化したリードを設けてある。すなわち、本実用例によれば、リードの位置のはば2/3がレジンにより埋め込まれ、その埋め込まれたリード一端面(上面)が半導体チップとの電気的接続部をなし、一方、リードの位置のはば1/3がレジンから突出、その突出した端面は実用部への接続端子、つまりカギリードとなる。

〔0030〕これにより、実用内における基板とカギリードの接続部分の形状を両端でどちらとしに、角型化パッケージが用られる。リードフレームに位置をつりなくてもよくなる。

〔0031〕図7に示す半導体部の形状は、前述の図1に示した半導体部の半導体チップ1上に自然端フィン6を設け、半導体チップから見せらる側を凸にしてやるものである。

〔0032〕なお、本実用新型は方を凸の半導体部をそれぞれ取り上げたが正方を凸のエンド部部についても

可である。

〔0033〕また、本実用新型のCOL(CHIP ON LEAD)部の半導体部は、既存からカギリードを取出せた物を取り上げたが、LOC(LEAD ON CHIP)部等の半導体部においては、上面からカギリードを取出せる。

〔0034〕したがって、半導体チップとそれに密接に接続された内部リードを封止して封止した半導体部であって、既存半導体部の封止部封止部の既存ししくは、上面から内部リードの一部を取出せることにより、半導体部の封止部封止部のうちも既存内に外部リードがあり、既存の外部リードの取出によって部分とされていた実用部は縮小できるので、半導体部の基部実用部における実用部を向上することが可能となる。

〔0035〕以上、本実用新によってなされた発明を、既存実用例によづて実用的に説明したが、本発明は、既存実用例に用いられるものでなく、その要旨を述及しない既存において既存可としてあることはむずである。

〔0036〕

(発明の図1) 本件において表示される発明のうち代表的なものによって示される実用部を既存に説明すれば、以下のとおりである。

〔0037〕半導体チップとそれに電気的に接続された内部リードを封止して封止した半導体部であって、既存半導体部の封止部封止部の既存ししくは、上面から内部リードの一部を取出せることにより、半導体部の封止部封止部のうちも既存内に外部リードがあり、既存の外部リードの取出によって部分とされていた実用部は縮小できるので、半導体部の基部実用部における実用部を向上することが可能となる。

(図1) (実用の一部実用である半導体部の構造を説明するための図である。

(図2) 本実用新型の半導体部の断面図である。

(図3) 本実用新型の半導体部の側面図である。

(図4) 本実用新型の半導体部の既存からみた半導体部である。

(図5) 本実用新型の半導体部におけるリードフレームの形状を説明するための図である。

(図6) 本実用新型の既存部である半導体部の構造を説明するための図である。

(図7) 本実用新型の既存部である半導体部の構造を説明するための図である。

(内号の説明)

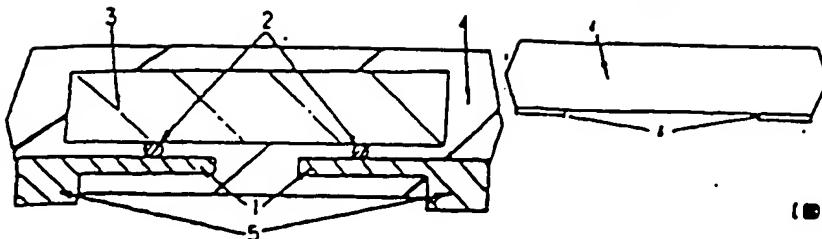
1…内部リード部分、2…パンプ、3…チップ、4…封止部、5…カギリード部分、6…自然端フィン。

(B1)

(B2)

图1

图2

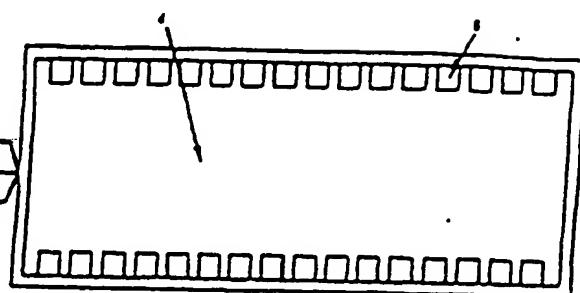
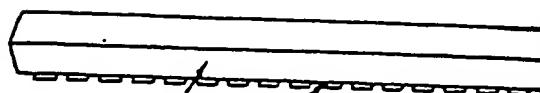


(B3)

图4

(B3)

图3

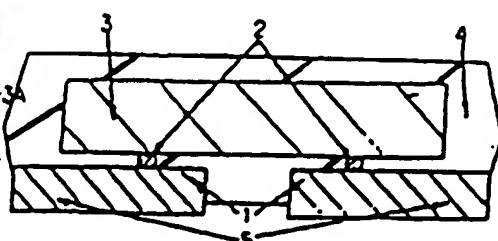
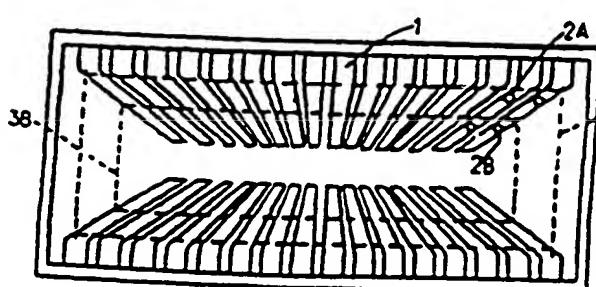


(B5)

(B6)

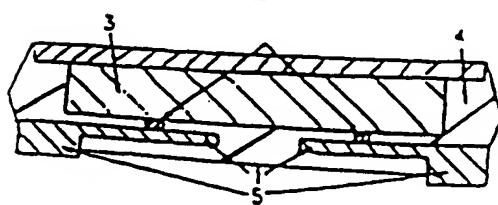
图5

图6



(B7)

图7



フロントページの記述

(81) Int. C.L.

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2010 11/30

技術監査室

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[TITLE OF THE INVENTION]

Semiconductor Device

5

[CLAIMS]

1. A semiconductor device including a semiconductor chip, inner leads electrically connected to the semiconductor chip, and a resin encapsulate adapted to encapsulate the semiconductor chip and the inner leads, wherein each of the inner leads is partially protruded from a lower surface or an upper surface of the resin encapsulate.
- 15 2. The semiconductor device in accordance with claim 1, wherein the inner leads are electrically connected to the semiconductor chip by bumps, respectively.
- 20 3. A semiconductor device including a semiconductor chip, a plurality of inner leads electrically connected to the semiconductor chip, and a resin encapsulate adapted to encapsulate the semiconductor chip and the inner leads, wherein each of the inner leads is encapsulated at a portion of the thickness thereof while being exposed at the remaining portion thereof in such a fashion that it has an
- 25

5 encapsulated main lead surface serving as an electrical connection to the semiconductor chip, and an exposed main lead surface positioned opposite to the encapsulated main lead surface, the exposed main lead surface serving as an outer lead.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

10 The present invention relates to a technique effective if applied to semiconductor devices.

[DESCRIPTION OF THE PRIOR ART]

15 In conventional semiconductor devices, a semiconductor chip is typically connected with inner leads by means of wires or bumps. Such a semiconductor device has a structure in which outer leads are laterally protruded from an encapsulate.

[SUBJECT MATTERS TO BE SOLVED BY THE INVENTION]

20 After reviewing the prior art, the inventors have found the following problems. A down-sizing of recent system appliances using semiconductor devices has resulted in a requirement to reduce the size of circuit boards on which semiconductor devices are mounted. To this end, 25 attempts to reduce the size of semiconductor devices have

been made in order to achieve an improvement in the mounting efficiency of circuit boards resulting in a reduction in the size of those circuit boards.

5 In most cases, such a reduction in the size of semiconductor devices have been achieved by reducing the size of semiconductor chips. For such a reduction in the size of semiconductor devices, outer leads have not been the subject of interest. That is, there has been no attempt to reduce the area occupied by outer leads of a 10 semiconductor device on a circuit board. Since conventional semiconductor devices have a structure in which outer leads are laterally protruded from a resin encapsulate, they have a mounting area increased by the area of the outer leads laterally protruded from the resin encapsulate. As a result, the conventional semiconductor devices involve a problem in that the mounting efficiency 15 thereof on a circuit board is degraded.

20 An object of the invention is to provide a technique capable of improving the mounting efficiency of a semiconductor device on a circuit board.

Other objects and novel features of the present invention will become more apparent after a reading of the following detailed description when taken in conjunction 25 with the drawings.

25

[MEANS FOR SOLVING THE SUBJECT MATTERS]

A representative of inventions disclosed in this application will now be summarized in brief.

30 In a semiconductor device in which a semiconductor chip and inner leads electrically connected to the semiconductor chip are encapsulated by resin, each of the

inner leads is partially protruded from a lower surface or
an upper surface of the resin encapsulate.

5 For a semiconductor device in which a semiconductor
chip and inner leads electrically connected to the
semiconductor chip are encapsulated by resin, the present
invention can improve the mounting efficiency of the
10 semiconductor device on a circuit board by protruding a
portion of each inner lead from the lower or upper surface
of the resin encapsulate in such a fashion that the outer
leads of the semiconductor device are received in an area
occupied by the resin encapsulate, thereby reducing the
15 mounting area of the outer leads by the area of outer leads
laterally protruded from a resin encapsulate in the case of
conventional semiconductor devices.

15 Now, the present invention will be described in
detail in conjunction with embodiments thereof.

20 In the drawings associated with the embodiments,
elements having the same function are denoted by the same
reference numeral, and repeated description thereof will be
omitted.

[EMBODIMENTS]

Fig. 1 is a view illustrating a semiconductor device
having a structure according to an embodiment of the
25 present invention. The semiconductor device according to
the embodiment of the present invention shown in Fig. 1 has
a rectangular structure. Fig. 2 is a side view of the
semiconductor device when viewed at the shorter side of the
rectangular structure. Fig. 3 is a side view of the
30 semiconductor device when viewed at the longer side of the
rectangular structure. Fig. 4 is a plan view of the
semiconductor device when viewed at the bottom.

In Figs. 1 to 4, the reference numeral 1 denotes

inner lead portions, 2 bumps, 3 a chip, 4 a resin encapsulate, and 5 outer lead portions, respectively.

As shown in Fig. 1, the semiconductor device of the present embodiment includes leads having a stepped lead structure. Each lead has an inner lead portion 1 serving as an inner lead, and an outer lead portion 5 serving as an outer lead.

The stepped lead structure can be obtained by half-etching the inner lead portions 1 of the leads. Alternatively, the stepped lead structure may be obtained by bonding two lead sheets to each other in such a fashion that they define a step therebetween, and then cutting the bonded lead sheets.

Within the resin encapsulate 4, bumps 2, which may be made of, for example, solder, are provided on the inner lead portions 1, respectively. Through these bumps 2, the inner lead portions are electrically connected to the semiconductor chip 3. Bumps previously provided at the semiconductor chip 3 may also be used as means for electrically connecting the inner lead portions 1 to the semiconductor chip 3. Alternatively, wires may be used.

As shown in Figs. 2 to 4, the outer lead portions 5, which are protruded from the resin encapsulate 4, are mounted on a circuit board or the like while being in surface contact with the circuit board. Accordingly, it is

possible to reduce the mounting space of the semiconductor device by the area of outer leads laterally protruded from a resin encapsulate in the case of conventional semiconductor devices. Otherwise, this area may be used to 5 mount other elements.

Now, a lead frame included in the semiconductor device according to the present embodiment will be described in conjunction with Fig. 5.

In Fig. 5, the reference numeral 3A denotes a larger 10 semiconductor chip, 3B a smaller semiconductor chip, 2A bumps for coupling inner leads to the larger semiconductor chip, and 2B bumps for coupling the inner leads to the smaller semiconductor chip, respectively.

As shown in Fig. 5, the lead frame of the 15 semiconductor device according to the present embodiment has a structure in which inner leads extend radially around an area near the center of the lead frame. Accordingly, any one of the semiconductor chips having different sizes, that is, the larger semiconductor chip 3A and smaller 20 semiconductor chip 3B indicated by phantom lines, can be connected with the inner lead portions 1 by shifting each pad position of the semiconductor chip 3A or 3B to a position where the semiconductor chip 3A or 3B can be connected to the inner leads 1, and providing a bump 2A or 25 2B at the shifted position. The electrical connection

between the inner leads and the semiconductor chip obtained by use of bumps as mentioned above provides an useful effect which cannot be expected in the case using wire connection. That is, one lead frame, which is configured in accordance with the present embodiment, can be applied to a variety of semiconductor chips.

Referring to Figs. 6 and 7, other embodiments of the present invention are illustrated, respectively.

In a semiconductor device according to the embodiment of Fig. 6, there is no step between the inner and outer lead portions 1 and 5 of each lead, as compared to the semiconductor device of Fig. 1. In this case, the semiconductor device includes leads each serving as both the inner and outer leads. In accordance with this embodiment, about 2/3 of the thickness of each lead is encapsulated by resin. One main surface of each lead, namely, the encapsulated main surface (upper surface), serves as an electrical connection to the semiconductor chip. About 1/3 of the thickness of each lead is exposed from the resin. The other main surface of each lead, namely, the exposed main surface, serves as a connection terminal to a mounting circuit board, for example, an outer lead.

In accordance with such a structure, it is possible to secure the area, where the outer leads can be connected

to the circuit board, upon the mounting of the semiconductor device. Furthermore, a thin package can be produced. In accordance with this embodiment, it is also unnecessary to provide a stepped lead structure for the

5 lead frame.

In a semiconductor device according to the embodiment of Fig. 7, radiation fins 6 are provided on the semiconductor chip 3 shown in Fig. 1 in order to radiate heat generated from the semiconductor chip 3.

10 Although the above embodiments have been described as being applied to rectangular semiconductor devices, they may also be applied to square semiconductor devices. Also, the above embodiments have been described as being applied to a semiconductor device having a COL (Chip On Lead) structure to protrude outer leads thereof from the lower surface of the encapsulate. In the case of a semiconductor device having an LOC (Lead On Chip) structure, outer leads thereof are protruded from the upper surface of the encapsulate.

15 20 For a semiconductor device in which a semiconductor chip and inner leads electrically connected to the semiconductor chip are encapsulated by resin, the present invention can improve the mounting efficiency of the semiconductor device on a circuit board by protruding a portion of each inner lead from the lower or upper surface

of the resin encapsulate in such a fashion that the outer leads of the semiconductor device are received in an area occupied by the resin encapsulate, thereby reducing the mounting area of the outer leads by the area of outer leads laterally protruded from a resin encapsulate in the case of conventional semiconductor devices.

Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

(EFFECTS OF THE INVENTION)

Effects obtained by a representative one of the inventions disclosed in this application will now be described in brief.

For a semiconductor device in which a semiconductor chip and inner leads electrically connected to the semiconductor chip are encapsulated by resin, the present invention can improve the mounting efficiency of the semiconductor device on a circuit board by protruding a portion of each inner lead from the lower or upper surface of the resin encapsulate in such a fashion that the outer leads of the semiconductor device are received in an area occupied by the resin encapsulate, thereby reducing the mounting area of the outer leads by the area of outer leads laterally protruded from a resin encapsulate in the case of conventional semiconductor devices.

CLIPPEDIMAGE= JP407297344A

PUB-NO: JP407297344A

DOCUMENT-IDENTIFIER: JP 07297344 A

TITLE: LEAD FRAME

PUBN-DATE: November 10, 1995

INVENTOR-INFORMATION:

NAME

UMEKI, AKIHIRO

INT-CL_(IPC): H01L023/50; H01L023/28

ABSTRACT:

PURPOSE: To prevent the warping of a die pad and the warping of a die-pad supporting pin, which occur when a dimple of the rear surface of the die pad is formed by press machining, by providing the curved part at the die-pad supporting pin, which is connected to the die pad and a lead frame.

CONSTITUTION: A die pad 1 is supported with a die-pad supporting pin 3 and connected to a lead frame 4. Then, a curved part 5 is formed at the approximately central part of the die-pad supporting pin 3 by curving the die-pad supporting pin 3. Then, the curved part 5 absorbs the stress in the horizontal direction and the stress in the vertical direction, which are applied when the die pad 1 undergoes press machining. Thus, the warping of the die pad and the warping of the die-pad supporting pin can be prevented.

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FPAR:

PURPOSE: To prevent the warping of a die pad and the warping of a die-pad supporting pin, which occur when a dimple of the rear surface of the die pad is formed by press machining, by providing the curved part at the die-pad supporting pin, which is connected to the die pad and a lead frame.

FPAR:

CONSTITUTION: A die pad 1 is supported with a die-pad supporting pin 3 and